(2-92)Sheet 1 of 1 Form PTO-1449 **Docket Number (Optional)** Application Numbe 0/ 3025.1US (95-1003.1) 09/506,204 INFORMATION DISCLOSUNE CITATIO Applicant Trung T. Doan IN AN APPLICATION PADEN Filing Date February 17, 2000 (Use several sheets if necessary) **U.S. PATENT DOCUMENTS** FILING DATE IF APPROPRIATE DOCUMENT **EXAMINER** DATE NAME CLASS SUBCLASS INITIAL NUMBER 5,527,561 06/1996 Dobson 5,985,763 11/1999 Hong et al. 5,998,296 12/1999 Saran et al. FOREIGN PATENT DOCUMENTS Translation DOCUMENT DATE COUNTRY CLASS SUBCLASS NUMBER **OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

**EXAMINER** 

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Sheet 1 of 1 Form PTO-1449 Docket Number (Optional) **Application Number** 3025.1US (95-1003.1) Nor Yer Assigned INFORMATION DISCLOSURE CITATION 09/506,204 Applicant Trung T. Doan IN AN APPLICATION (Use several sheets if necessary) Filing Date February 17, 2000 Group Art Unit Unknown-**U.S. PATENT DOCUMENTS EXAMINER** DOCUMENT FILING DATE DATE NAME CLASS SUBCLASS INITIAL NUMBER IF APPROPRIATE 257 741 5,355,020 10/11/94 Lee et al. 5,512,512 04/30/96 Isobe FOREIGN PATENT DOCUMENTS DOCUMENT NUMBER DATE COUNTRY CLASS SUBCLASS OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) Dixit et al., "A Novel High Pressure Low Temperature Aluminum Plug Technology For Sub-0.5, µm Contact/Via Geometries", IEDM, pp. 105-108, 1994. | Dec. 1994, pp. 105-108 Dixit et al., "A Novel 0.25  $\mu$ m Via Plug Process Using Low Temperature CVD AI/TiN", IEDM 95, pp. 1001-1003. Dixit et al., "A reactively sputtered coherent TiN process for sub-0.5 µm technology", SPIE, Vol. 2090 Multilevel Interconnection; pp. 12-21, 1993. Dixit et al., "An Integrated Low Resistance Aluminum Plug and Low-k Polymer Dielectric For High Performance 0.25 µm Interconnects", 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 86-87, 1996. Dixit et al., "Application of High Pressure Extruded Aluminum to ULSI Metallization", Semiconductor International, pp. 79-85, August 1995. Jain et al., "Chemical mechanical planarization of multilayer dielectric stacks", SPIE, Vol. 2335, pp. 2-11, 193. Mizobuchi et al., "Application of Force Fill Al-Plug Technology to 64Mb DRAM and 0.35 µm Logic", 1995 Symposium on VLSI Technology Digest of Technical Papers", 45-46. Ting et al., "Effect of Via Etch Profile and Barrier Metal on Electromigration Performance of Wfilled Via Structure in TiN/A1Cu/TiN Metallization", Mat. Res. Soc. Symp. Proc., Vol. 391, pp. 453-458, 1995. DATE CONSIDERED 1/03/1200 **EXAMINER** Kuach EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through

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